

1 In the claims:

- 2 1. A bi-directional high speed video data transmission system, comprising:
3 a transmitter operative to receive and transmit a first video data stream;
4 a data pair connected to the transmitter, operative to relay the first video data
5 stream from the transmitter;
6 a receiver connected to the data pair and operative to receive the first video data
7 stream relayed by the data pair;
8 a first and second summing resistor connected to the data pair, the first and second
9 summing resistor operative to convert a current transmitted across the data pair to a DC
10 return current;
11 a return transmitter connected to the first and second summing resistor and
12 operative to receive the DC return current and a return video data stream, further
13 operative to transmit the return video data stream;
14 a return data pair connected to the return transmitter, operative to relay the return
15 serial video data stream from the transmitter; and
16 a return receiver connected to the return data pair and operative to receive the
17 return video serial data stream, the return receiver further connected to the transmitter.
- 18 2. The bi-directional high speed video data transmission system of claim 1, wherein:
19 the data pair comprises a first and second data line;
20 the return data pair comprises a first and second return data line;
21 the transmitter transmits the first video data stream by switching a DC-balanced
22 current between the first and second data line, thus creating a first and second AC current
23 on the first and second data line;
24 the first and second summing resistor convert the current transmitted across the
25 data pair to a DC return current by merging the first AC current with the second AC
26 current; and
27 the return transmitter transmits the return video data stream by switching the DC
28 return current between the first and second return data line, thus creating a first and
29 second AC return current on the first and second return data line.
- 30 3. The bi-directional high speed video data transmission system of claim 2, further
31 comprising a filter connected between the first and second summing resistor and the
32 return transmitter.
- 33 4. The bi-directional high speed video data transmission system of claim 3, wherein
34 the filter eliminates line noise present in the DC return current.

1 5. The bi-directional high speed video data transmission system of claim 3, wherein
2 the filter is an LC filter.

3 6. The bi-directional high speed video data transmission system of claim 2, further
4 comprising:

5 a first clock signal having a regularly repeating digital clock pulse;
6 the transmitter operative to regulate the switching of the DC-balanced current
7 between the first and second data line according to the digital state of the clock pulse; and
8 the return transmitter operative to regulate the switching of the DC return current
9 between the first and second return data line according to the digital state of the clock
10 pulse.

11 7. The bi-directional high speed video data transmission system of claim 2, further
12 comprising:

13 a first clock signal having a first period;
14 the transmitter further operative to regulate the switching of the DC-balanced
15 current between the first and second data line according to the digital state of the first
16 clock pulse;
17 a second clock signal having a second period of different duration than the first
18 period;
19 the return transmitter further operative to regulate the switching of the DC return
20 current between the first and second return data line according to the digital state of the
21 clock pulse.

22 8. The bi-directional high speed video data transmission system of claim 6, wherein:
23 the transmitter regulates the switching of the DC-balanced current between the
24 first and second data line by switching the DC-balanced current at a time corresponding
25 to a first edge of the clock pulse; and

26 the return transmitter regulates the switching of the DC return current between the
27 first and second data line by switching the DC return current at a time corresponding to a
28 second edge of the clock pulse.

29 9. A video camera incorporating the bi-directional high speed video data
30 transmission system of claim 2.

31 10. A computer video system incorporating the bi-directional high speed video data
32 transmission system of claim 2.

33 11. The bi-directional high speed video data transmission system of claim 2, further
34 comprising a first and second return summing resistor connected between the return data

1 pair and the transmitter, the first and second return summing resistor operative to merge
2 the AC current transmitted across the first return data line with the AC current transmitted
3 across the second data line into a DC current.

4 12. The bi-directional high speed video data transmission system of claim 11,
5 wherein:

6 the transmitter, return receiver, and first and second return summing resistor
7 comprise a first transceiver;

8 the return transmitter, receiver, and first and second summing resistor comprise a
9 second transceiver; and

10 the circuitry of the first and second transceivers are identical.

11 13. A unidirectional high speed video data transmission system, comprising:

12 a first transition minimized differential signaling transmitter operative to transmit
13 a first video data stream by alternating a DC current between a first and second data line;

14 a data pair comprised of the first and second data line and having a first and
15 second end, the data pair connected to the first transition-minimized differential signaling
16 transmitter at the first end, the data pair further connected to a first transition-minimized
17 differential signaling receiver at the second end, the data pair operative to relay the first
18 video data stream from the first transmitter to the first receiver;

19 the first transition-minimized differential signaling receiver operative to receive
20 and output the first video data stream;

21 a first summing resistor connected to the first data line;

22 a second summing resistor connected to the second data line;

23 the first and second summing resistors comprising a first summing pair operative
24 to merge the alternating current across the first and second data lines to form a DC return
25 current;

26 a second transition minimized differential signaling transmitter operative to
27 transmit a second video data stream by alternating a second DC current between a third
28 and fourth data line;

29 a second data pair comprised of the third and fourth data line and having a first
30 and second end, the second data pair connected to the second transition-minimized
31 differential signaling transmitter at the first end, the second data pair further connected to
32 a second transition-minimized differential signaling receiver at the second end, the second
33 data pair operative to relay the second video data stream from the second transmitter to
34 the second receiver;

1 the second transition-minimized differential signaling receiver operative to receive
2 and output the second video data stream;
3 a third summing resistor connected to the third data line;
4 a fourth summing resistor connected to the fourth data line;
5 the third and fourth summing resistors comprising a second summing pair
6 operative to merge the alternating current across the third and fourth data lines to form a
7 DC final current;
8 wherein the DC return current and the second DC current are the same; and
9 wherein the third data line functions as a DC return channel.

10 14. The unidirectional high speed video data transmission system of claim 13, further
11 comprising:
12 a clock signal having a regularly repeating digital clock pulse;
13 the first transition-minimized differential signaling transmitter operative to
14 regulate the switching of the DC current between the first and second data line according
15 to the digital state of the clock pulse; and
16 the second transition-minimized differential signaling transmitter operative to
17 regulate the switching of the DC return current between the first and second return data
18 line according to the digital state of the clock pulse.

19 15. The unidirectional high speed video data transmission system of claim 14,
20 wherein:
21 the first transition-minimized differential signaling transmitter regulates the
22 switching of the DC current between the first and second data line by switching the DC
23 current at a time corresponding to a first edge of the clock pulse; and
24 the second transition-minimized differential signaling transmitter regulates the
25 switching of the DC return current between the first and second data line by switching the
26 DC return current at a time corresponding to a second edge of the clock pulse.

27 16. The unidirectional high speed video data transmission system of claim 15, further
28 comprising a filter located between the first and second summing pairs, the filter
29 operative to minimize line noise in the video data transmission system.

30 17. A method for enabling bi-directional high speed video data transmission,
31 comprising the steps of:
32 receiving a parallel video data signal;
33 receiving a DC input current;
34 encoding the parallel video data signal as a serial video data signal;

1 transmitting the serial video data signal across a first and second data line by
2 alternately transferring the DC input current between a first data line and a second data
3 line to yield a first and second current, the first and second currents alternating between
4 zero and a fixed value, the first and second currents one hundred eighty degrees out of
5 phase with one another;
6 receiving the serial video data signal;
7 decoding the serial video data signal into the parallel video data signal;
8 summing the first and second currents into a DC return current;
9 receiving a return parallel video data signal;
10 encoding the return parallel video data signal as a return serial video data signal;
11 transmitting the return serial video data signal across a first and second return
12 data line by alternating the DC return current across the first and second return data lines
13 to yield a first and second return current, the first and second return currents alternating
14 between zero and a fixed value, the first and second return currents one hundred eighty
15 degrees out of phase with one another;
16 receiving the return serial video data signal; and
17 decoding the return serial video data signal into the return parallel video data
18 signal.
19 18. The method of claim 17, further comprising the step of, in response to summing
20 the first and second currents into a DC return current, filtering line noise from the DC
21 return current.
22 19. The method of claim 17, further comprising the steps of:
23 summing the first and second return currents into a DC loop current; and
24 using the DC loop current as the DC input current.
25 20. The method of claim 17, further comprising the steps of:
26 receiving a clock signal having a rising edge and falling edge;
27 in response to receiving the rising edge of the clock signal, alternating the DC
28 input current across the first and second data lines; and
29 in response to receiving the falling edge of the clock signal, alternating the DC
30 return current across the first and second return data lines.